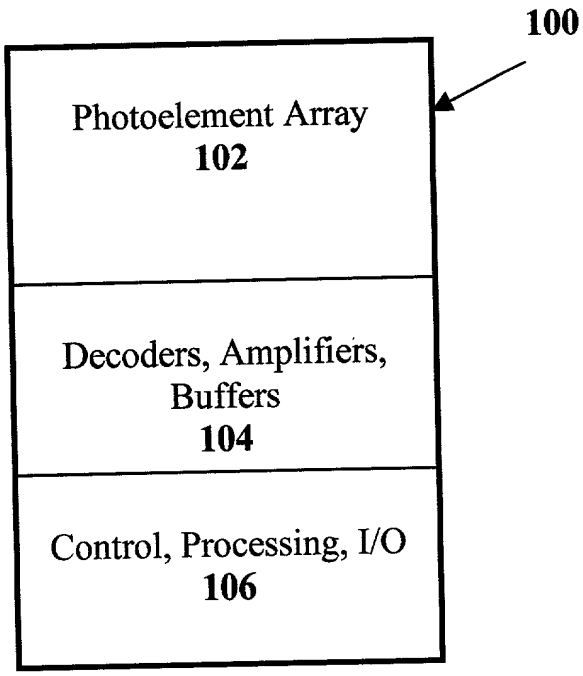

Figure 1
(prior art)

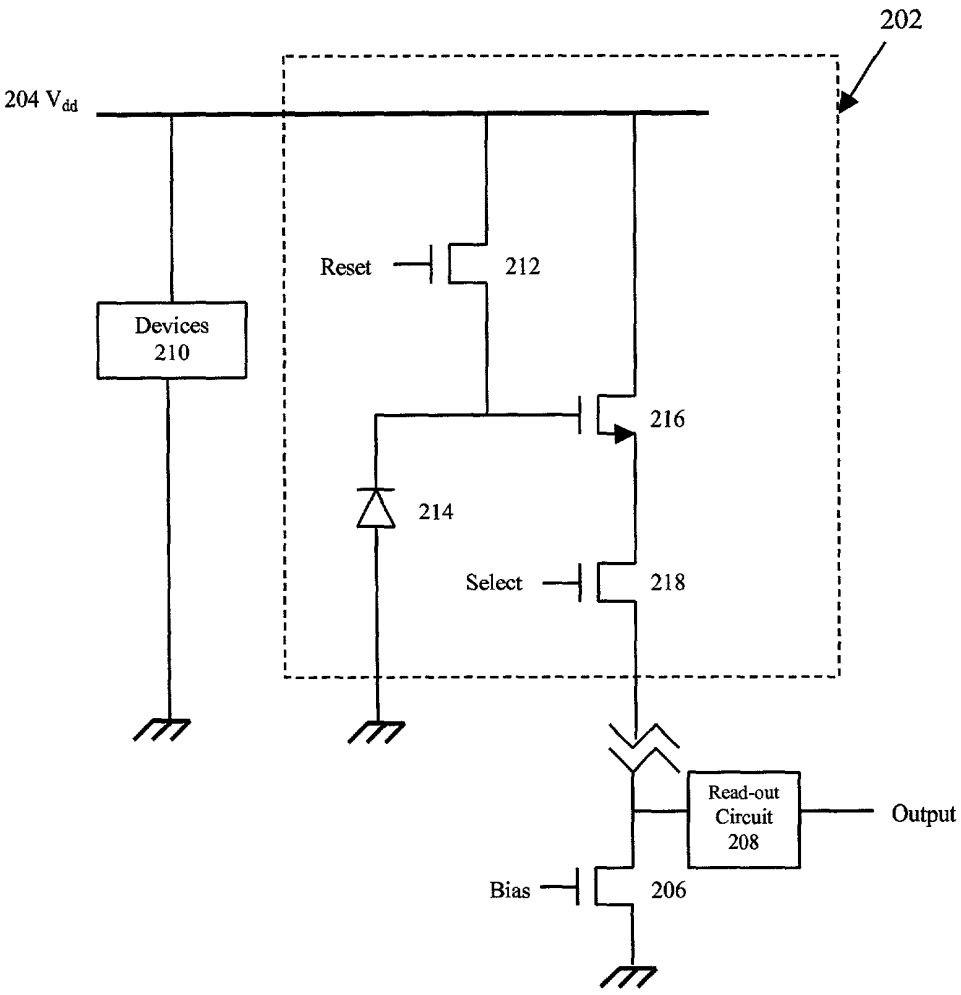

Figure 2
(prior art)

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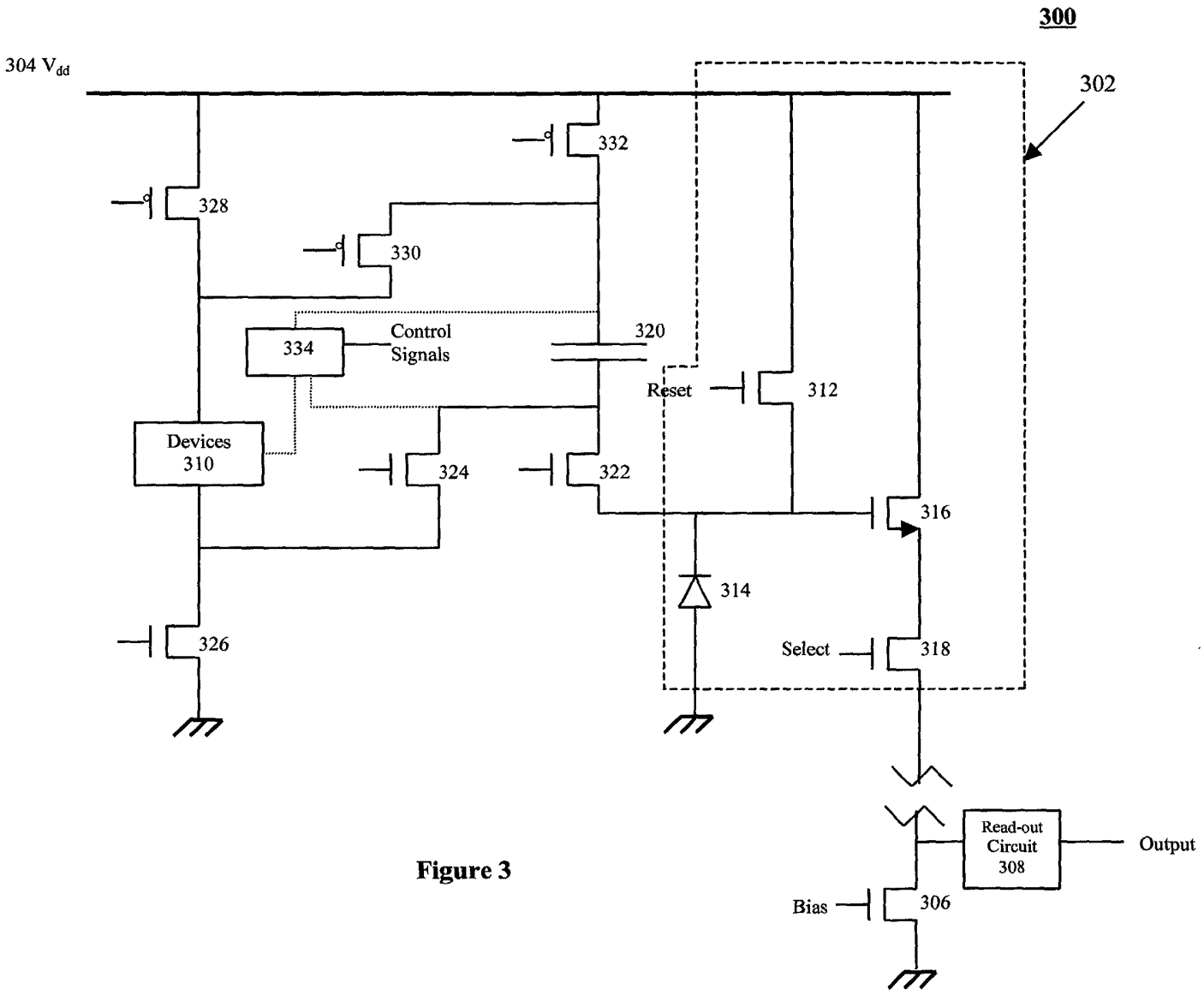
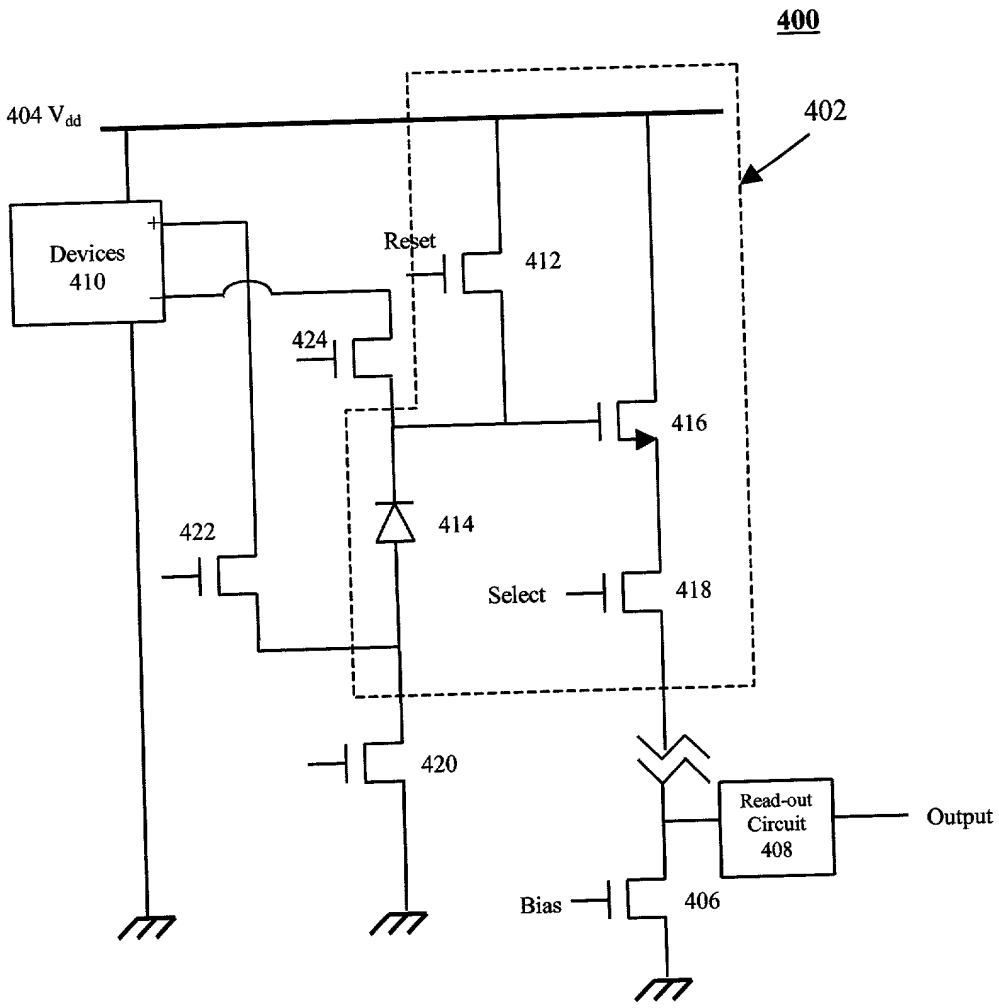


Figure 3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404 V_{dd}
402
Devices
410
Reset
412
424
416
414
422
Select
418
420
Read-out
Circuit
408
Output
Bias
406

Figure 4